The following listing of claims will replace all prior versions, and listing of

claims in the application:

Listing of Claims:

1. (Currently Amended) A single crystal oscillator RF transmitter system

comprising:

a microprocessor having a control signal output and a data output for

output of digital data to be transmitted;

a converter coupled to said microprocessor data output for

converting the digital data output from the microprocessor into digital packet data

to be transmitted by the system;

an external crystal oscillator;

a local oscillator responsive to an receiving a frequency signal from

the external crystal for oscillator and generating a first clock signal having a

frequency in a radio frequency band responsively to said external crystal oscillator

frequency signal;

a clock switch coupled to the local oscillator for providing a second

clock signal at a lower frequency than the first clock signal to the microprocessor

and a third clock signal to the converter, the third clock signal being a different

frequency than the first clock signal and the second clock signal, the clock switch

Page 2 of 21

Serial Number: 10/761,340

Reply to Office Action dated 30 July 2007

having an input coupled to the control signal output of the microprocessor for

receiving a command therefrom to start the local oscillator to generate the first

clock signal; and

a transmitter connected to an output of the converter for receiving

the digital packet data and being coupled to the local oscillator for use of the first

clock signal as an RF carrier for the digital packet data to be transmitted by the

transmitter:

wherein the microprocessor, converter, local oscillator, clock switch

and transmitter are integrated on a chip.

2. (Previously Presented) The system of claim 1, wherein the clock switch

comprises a frequency divider for frequency-dividing the first clock signal to

generate the second clock signal.

3. (Previously Presented) The system of claim 1, wherein the clock switch

comprises a frequency divider for frequency-dividing the first clock signal to

generate the third clock signal.

4. (Previously Presented) The system of claim 1, further comprising an RC

oscillator for generating the second clock signal.

Page 3 of 21

Serial Number: 10/761,340

Reply to Office Action dated 30 July 2007

5. (Previously Presented) The system of claim 4, wherein the clock switch

comprises a frequency divider for frequency-dividing the first clock signal to

generate the third clock signal.

6. (Previously Presented) The system of claim 4, wherein the RC oscillator

is connected with an external resistor for tuning the second clock signal.

7. (Original) The system of claim 6, wherein the external resistor comprises

a variable resistor.

8. (Previously Presented) The system of claim 4, wherein the RC oscillator

comprises a resistor network for determining the second clock signal.

9. (Previously Presented) The system of claim 4, wherein the

microprocessor signals the local oscillator to turn off after the digital packet data is

transmitted.

10. (Previously Presented) The system of claim 4, wherein the converter

and transmitter signal the local oscillator to turn off after the digital packet data is

transmitted.

Page 4 of 21

Serial Number: 10/761,340

Reply to Office Action dated 30 July 2007

11. (Original) The system of claim 1, further comprising a peripheral circuit

connected to the microprocessor.

12. (Cancelled).

13. (Cancelled).

14. (Currently Amended) A method for transmitting data with an RF

transmitter system having a single crystal oscillator and including a

microprocessor connected with a converter that is further in turn connected to a

transmitter, the method comprising the steps of:

receiving at a local oscillator a frequency signal from an external

crystal oscillator;

generating at said local oscillator a first clock signal at a radio

frequency with a responsive to the external crystal oscillator frequency signal for

providing to the transmitter a carrier signal responsive to upon receipt of a control

signal from the microprocessor to start generation of the first clock signal;

generating a second clock signal and a third clock signal by dividing

down the first clock signal for respectively providing to the microprocessor and

converter clock signals of respectively reduced frequency;

converting digital data output from the microprocessor into digital

Page 5 of 21

Serial Number: 10/761,340

Reply to Office Action dated 30 July 2007

packet data by the converter for output to the transmitter; and

transmitting the digital packet data modulated on the first clock

signal.

15. (Cancelled).

16. (Currently Amended) A method for transmitting data with an RF

transmitter system having a single crystal oscillator and including a

microprocessor connected with a converter that is in turn connected to a

transmitter, the method comprising the steps of:

receiving at a local oscillator a frequency signal from an external

crystal oscillator;

generating at said local oscillator a first clock signal at a radio

frequency with a responsive to the external crystal oscillator frequency signal

responsive to upon receipt of a control signal from the microprocessor to start

generation of the first clock signal;

generating a second clock signal using an RC oscillator;

generating a third clock signal from the first clock signal output from

the erystal local oscillator for coupling to the converter, the third clock frequency

being a lower frequency than a frequency of the first clock signal;

generating a fourth clock signal from the second clock signal for

Page 6 of 21

Serial Number: 10/761,340

Reply to Office Action dated 30 July 2007

coupling to the microprocessor, said fourth clock signal being a lower frequency

than the frequency of the first clock signal and being a higher frequency than the

third clock signal;

outputting digital data from the microprocessor for transmission by

the transmitter;

converting the digital data output from the microprocessor into

digital packet data by the converter; and

modulating the digital packet data with the first clock signal in the

transmitter for transmitting an RF signal therefrom.

17. (Previously Presented) The method of claim 16, wherein the step of

generating a fourth clock signal from the second clock signal comprises the step of

frequency-dividing the second clock signal.

18. (Previously Presented) The method of claim 16, further comprising the

step of tuning an external resistor connected to the RC oscillator for determining

the oscillator output signal.

19. (Previously Presented) The method of claim 16, further comprising the

step of trimming a built-in resistor network connected to the RC oscillator for

determining a frequency of the oscillator output signal.

Page 7 of 21

Serial Number: 10/761,340

Reply to Office Action dated 30 July 2007

20. (Previously Presented) The method of claim 16, further comprising the

step of the microprocessor signaling the crystal oscillator to stop generating the

first clock signal after the RF signal is transmitted.

21. (Previously Presented) The method of claim 16, further comprising the

step of the microprocessor signaling the converter to turn off after the RF signal is

transmitted.

22. (Previously Presented) The method of claim 16, further comprising the

step of the microprocessor signaling the transmitter to turn off after the RF signal

is transmitted.